CLAIMS:

1. A method of forming a semiconductor construction, comprising:

forming a first substrate comprising silicon-containing structures separated from one another by an insulative material; the silicon-containing structures defining an upper surface;

forming a second semiconductor substrate comprising a monocrystalline material having a damage region therein;

bonding the second semiconductor substrate to the silicon-containing structures at the upper surface; and

cleaving the monocrystalline material along the damage region.

2. The method of claim 1 wherein the cleaving leaves a rough upper surface of the monocrystalline material over the silicon-containing structures; and further comprising, after the cleaving, smoothing the upper surface of the monocrystalline material.

3. The method of claim 1 wherein the silicon-containing structures comprise conductively-doped silicon.

4. The method of claim 1 wherein the silicon-containing structures comprise amorphous silicon.

5. The method of claim 1 wherein the silicon-containing structures comprise polycrystalline silicon.

6. The method of claim 1 wherein the silicon-containing structures comprise monocrystalline silicon.

7. A method of forming a semiconductor construction, comprising:

forming a first semiconductor substrate comprising a first monocrystalline base and having a first transistor supported on the first monocrystalline base; the first transistor having source/drain regions associated therewith; the first substrate also having an insulative material formed over the base and silicon-containing plugs extending through the insulative material and to the source/drain regions; the silicon-containing plugs being separated from one another by the insulative material and defining a planarized upper surface above the first monocrystalline base;

providing a second semiconductor substrate comprising a second monocrystalline base and bonding the second semiconductor substrate to the silicon-containing plugs at the planarized upper surface above the first monocrystalline base; and

forming a second transistor supported over the second substrate.

8. The method of claim 7 wherein one of the first and second transistors is a PMOS transistor and wherein the other of the first and second transistors is an NMOS transistor.

9. The method of claim 7 wherein the second transistor comprises source/drain regions which extend entirely through the second monocrystalline base.

10. The method of claim 7 wherein the second transistor comprises source/drain regions which extend only partially through the second monocrystalline base.

11. A method of forming a semiconductor construction, comprising:

forming a first semiconductor substrate comprising a first monocrystalline base and silicon-containing structures above the base, at least some of the silicon-containing structures being separated from one another by an insulative material; the silicon-containing structures and insulative material together defining a planarized upper surface above the first monocrystalline base;

forming a second semiconductor substrate comprising a second monocrystalline base and having a damage region formed within the second monocrystalline base;

bonding the second semiconductor substrate to the silicon-containing structures at the planarized upper surface above the first monocrystalline base; and

cleaving the second monocrystalline base along the damage region.

12. The method of claim 11 the first and second monocrystalline bases comprise monocrystalline silicon.

13. The method of claim 11 wherein some of the silicon-containing structures have no function except to bond to the second semiconductor substrate; and wherein others of the silicon-containing structures have additional functions besides bonding to the second semiconductor substrate.

14. The method of claim 11 wherein the second monocrystalline base is bonded to the silicon-containing structures.

15. The method of claim 11 wherein the bonding the second semiconductor structure comprises bonding the second monocrystalline base to the silicon-containing structures, and bonding the second monocrystalline base to the insulative material at the planarized upper surface above the first monocrystalline base.

16. The method of claim 11 wherein the damage region is formed by implanting hydrogen ions into the second monocrystalline base.

17. The method of claim 11 wherein the damage region is formed by implanting hydrogen ions into the second monocrystalline base, and wherein the cleaving comprise thermally treating the second monocrystalline base.

18. The method of claim 11 wherein the only temperatures utilized for the bonding are less than or equal to about 700°C, and further comprising not exposing the first monocrystalline base to temperatures exceeding 700°C after the bonding.

19. The method of claim 11 further comprising forming at least one doped silicon region extending through the second monocrystalline base and electrically contacting at least one of the silicon-containing structures.

20. The method of claim 11 further comprising:

forming at least one doped silicon region extending through the second monocrystalline base and electrically contacting at least one of the silicon-containing structures; and

forming at least one other doped silicon region within the second monocrystalline base, but which does not extend entirely through the second monocrystalline base.

21. A method of forming a semiconductor construction, comprising:

forming a first substrate comprising silicon-containing structures separated from one another by an insulative material; the silicon-containing structures defining an upper surface;

bonding a second semiconductor substrate to the silicon-containing structures at the upper surface; the second semiconductor substrate comprising a monocrystalline material which is bonded to the silicon-containing structures; and

forming at least one doped silicon region extending through the monocrystalline material and electrically contacting at least one of the silicon-containing structures.

22. The method of claim 21 wherein the forming the at least one doped silicon region comprises implanting dopant into the monocrystalline material.

23. The method of claim 21 further comprising forming at least one insulative region extending at least partially into the monocrystalline material.

24. The method of claim 21 further comprising forming at least one insulative region extending through the monocrystalline material.

25. The method of claim 24 wherein the forming the at least one insulative region comprises:

forming an opening through the monocrystalline material; and

filling the opening with an insulative material.

26. The method of claim 21 wherein the forming the at least one doped silicon region comprises:

forming an opening through the monocrystalline material; and

filling the opening with a doped silicon material.

27. The method of claim 26 wherein the doped silicon material comprises doped amorphous silicon.

28. The method of claim 26 wherein the doped silicon material comprises doped polycrystalline silicon.

29. The method of claim 21 further comprising forming at least one second doped silicon region within the second monocrystalline base and which does not extend entirely through the second monocrystalline base.

30. The method of claim 29 wherein the forming the at least one doped silicon region comprises:

forming an opening through the monocrystalline material; and

filling the opening with a doped silicon material.

31. The method of claim 30 wherein the doped silicon material comprises doped amorphous silicon.

32. The method of claim 30 wherein the doped silicon material comprises doped polycrystalline silicon.

33. A semiconductor construction, comprising:

a first substrate comprising silicon-containing structures separated from one another by an insulative material; the silicon-containing structures defining an upper surface; and

a second semiconductor substrate comprising a monocrystalline material bonded over the silicon-containing structures at the upper surface.

34. The construction of claim 33 further comprising one of either a PMOS or NMOS transistor having a gate between the first and second substrates; and the other of a PMOS or NMOS transistor having a gate over the second substrate.

35. The construction of claim 33 further comprising only one type of PMOS type or NMOS type transistors having a gate between the first and second substrates; and the other type PMOS type and NMOS type transistors having a gate over the second substrate.

36. The construction of claim 33 further comprising only one type of PMOS type or NMOS type transistors having a gate between the first and second substrates; and both types of PMOS type and NMOS type transistors having gates over the second substrate.

37. The construction of claim 33 further comprising both types of PMOS type and NMOS type transistors having gates between the first and second substrates; and only one type of the PMOS type and NMOS type transistors having a gate over the second substrate.

38. The construction of claim 33 wherein the monocrystalline material of the second semiconductor substrate is monocrystalline silicon.

39. The construction of claim 33 wherein the silicon-containing structures comprise conductively-doped silicon.

40. The construction of claim 33 wherein the silicon-containing structures comprise amorphous silicon.

41. The construction of claim 33 wherein the silicon-containing structures comprise polycrystalline silicon.

42. The construction of claim 33 wherein the silicon-containing structures comprise monocrystalline silicon.

43. A semiconductor construction, comprising:

a first semiconductor substrate comprising a first monocrystalline base and silicon-containing structures above the base, at least some of the silicon-containing structures being separated from one another by an insulative material; the silicon-containing structures and insulative material together defining an upper surface above the first monocrystalline base; and

a second semiconductor substrate comprising a second monocrystalline base bonded to the silicon-containing structures at the upper surface above the first monocrystalline base.

44. The construction of claim 40 the first and second monocrystalline bases comprise monocrystalline silicon.

45. The construction of claim 40 wherein the second monocrystalline base is bonded to the insulative material at the upper surface above the first monocrystalline base.

46. The construction of claim 40 further comprising at least one electrically insulative region extending through the second monocrystalline base.

47. The construction of claim 40 further comprising at least one doped silicon region extending through the second monocrystalline base and electrically contacting at least one of the silicon-containing structures.

48. The construction of claim 40 further comprising:

at least one doped silicon region extending through the second monocrystalline base and electrically contacting at least one of the silicon-containing structures; and

at least one insulative region extending through the second monocrystalline base.

49. The construction of claim 40 further comprising:

at least one doped silicon region extending through the second monocrystalline base and electrically contacting at least one of the silicon-containing structures; and

at least one doped silicon region within the second monocrystalline base, but which does not extend entirely through the second monocrystalline base.